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STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

| EXAMINER | |
|---|---|
| SELBY, GEVELL V | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2615 | |

DATE MAILED: 09/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/775,639 | OGAWA, YOSHIMASA | |
| | Examiner | Art Unit | |
| | Gevell Selby | 2615 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-26 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-26 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 05 February 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Specification*

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

Claims 4 and 11 recite the limitation "second" in line 2. There is insufficient antecedent basis for this limitation in the claim. There is no first switch circuit claimed is this claim or the independent claim. For examination purposes, the word "second " will be omitted from the claim.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**4. Claims 1-7, 18, 19, 21, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Hirota, US 5,291, 294.**

In regard to claim 1, Hirota, US 5,291, 294, discloses a solid-state imaging element, comprising:

a plurality of light-receiving sensors (see figure 8, element 32) converting optical signals to electrical signals (see column 6, lines 30-33); and

a memory (see figure 8, element 36) storing the electrical signals as optical image data, said memory being formed of a plurality of line buffers (see column 6, lines 47-49).

In regard to claim 2, Hirota, US 5,291, 294, discloses the solid-state imaging element of claim 1, further comprising:

a first switch circuit connecting one of the line buffers and said light-receiving sensors (see column 6, lines 49-53).

In regard to claim 3, Hirota, US 5,291, 294, discloses the solid-state imaging element of claim 2, wherein the data in the line buffers are output in parallel (see column 6, lines 60-62).

In regard to claim 4, Hirota, US 5,291, 294, discloses the solid-state imaging element of claim 1 comprising:

a switch circuit selecting one of the line buffers to output the electrical signal (see column 6, lines 60-63: It is inherent that there are switches to control the flow of the signals from each register to the transfer section).

In regard to claim 5, Hirota, US 5,291, 294, discloses a solid-state imaging element, comprising:

a plurality of light receiving sensors (see figure 4, element 32) arranged as m sensors in each of n lines to convert optical signals to electrical signals (see column 6, lines 30-33); and

a memory (see figure 8, element 36) storing the electrical signals as optical image data, said memory being formed of a plurality of buffers, each buffer storing m data (see column 6, lines 47-49).

In regard to claim 6, Hirota, US 5,291, 294, discloses the solid-state imaging element of claim 5, further comprising:

a switch circuit connecting one of the buffers and said light-receiving sensors (see column 6, lines 49-53).

In regard to claim 7, Hirota, US 5,291, 294, discloses the solid-state imaging element of claim 6, further comprising:

a transfer control circuit (see figure 8, element 33) selecting certain ones of said light-receiving sensors to supply the electrical signal to the buffers (see column 6, lines 48-42).

In regard to claims 18 and 24, Hirota, US 5,291, 294, discloses a charge-coupled device (CCD) and the method of outputting image data from the CCD, comprising:

a vertical CCD (see figure 9, element 41) having a plurality of photosensors arranged in v vertical lines and n horizontal lines corresponding to an n.times.v frame of pixels, and converting optical signals to electrical signal image data (see column 7, lines 30-47: When the image senor is rotated by 90 degrees, the element 33 can be read as the Vertical CCD and element 34 as the horizontal CCD);

a horizontal CCD (see figure 9, element 44) having n line buffers (see figure 9, element 47), each buffer holding up to v pixels of image data (see column 7, lines 48-51);

a first switch circuit connected to each of the vertical lines and the line buffers (see column 7, lines 39-47);

a first switch control circuit controlling said first switch circuit so that each line buffer sequentially connects to said vertical CCD, the image data in sequential ones of the n horizontal lines of said vertical CCD being transferred to a corresponding one of the n line buffers (see column 7, lines 39-47);

a second switch circuit connected to the line buffers and an external circuit (see column 8, lines 3-8); and

a second switch control circuit controlling said second switch circuit so that each line buffer sequentially connects to the external circuit, the image data in the line buffers being transferred to the external circuit in blocks of n.times.m (m<v) pixels, each line buffer in each block transferring m pixels (see column 8, lines 3-8).

In regard to claim 19, Hirota, US 5,291, 294, discloses a charge-coupled device (CCD), comprising:

a vertical CCD (see figure 9, element 41) having a plurality of photosensors arranged in v vertical lines and n horizontal lines corresponding to an n.times.v frame of pixels, each horizontal line being divided into k line sections, each line section corresponding to m (m<k) pixels of image data (The

number of sections equals the number of columns), and converting optical signals to electrical signal image data (see column 7, lines 30-47: When the image senor is rotated by 90 degrees, the element 33 can be read as the Vertical CCD and element 34 as the horizontal CCD);

a horizontal CCD (see figure 9, element 44) having k line buffers (see figure 9, element 47) connected to an external circuit, each line buffer holding up to m pixels of image data (see column 7, lines 48-51);

a switch circuit connected to the line buffers and the external circuit (see column 7, lines 39-47);

a transfer control circuit controlling said vertical CCD such that blocks of n.times.m pixels of image data are transferred from said vertical CCD to the line buffers, wherein a first one of the buffers receives m pixels from a horizontal line and outputs the m pixels to the external circuit before receiving another m pixels from the next horizontal line and so forth until a first block of n.times.m pixels has been transferred and output, and repeating the transfer and output operations for each remaining line buffer and the remaining image data (see column 7, lines 39-47); and

a switch control circuit controlling said switch circuit so that each line buffer sequentially connects to the external circuit to output the image data to the external circuit (see column 8, lines 3-8).

In regard to claim 21, Hirota, US 5,291, 294, discloses a charge-coupled device (CCD), comprising:

an array of photosensors arranged in v vertical lines and n horizontal lines corresponding to an n.times.v pixel array of image data (see figure 9, element 41 and column 7, lines 30-47: When the image senor is rotated by 90 degrees, the element 33 can be read as the Vertical CCD and element 34 as the horizontal CCD); and

a plurality of n line buffers (see figure 9, element 47), each line buffer holding up to v pixels of image data, wherein each line buffer sequentially connecting to said array, the image data in sequential ones of the n horizontal lines of said array being transferred to a corresponding one of the n line buffers (see column 7, lines 48-67), and each line buffer sequentially outputting the image data, the image data in the line buffers being output in blocks of n.times.m (m<v) pixels, each line buffer in each block outputting m pixels (see column 8, lines 2-8).

**5. Claims 22 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Morimoto, 5,969,759.**

In regard to claims 22 and 25, Morimoto, 5,969,759 discloses a charge-coupled device (CCD) and the method of outputting image data from the CCD, comprising:

an array of photosensors (see figure 3) arranged in v vertical lines and horizontal lines corresponding to an n.times.v pixel array of image data (see column 5, lines 9-16), each horizontal line being divided into k line sections, each line section corresponding to m (m<k) pixels of image data (see column 5, lines 16-21); and

a plurality of k line buffers (see figure 3, element 102a-d), each line buffer holding up to m pixels of image data, wherein blocks of n.times.m pixels of image data are transferred from the array of photosensors to the line buffers, such that a first one of the buffers receives m pixels from a horizontal line and outputs the m pixels before receiving another m pixels from the next horizontal line and so forth until a first block of n.times.m pixels has been transferred and output, and repeating the transfer and output operations for each remaining line buffer and the remaining image data (see column 7, lines 8-27).

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**7. Claims 8-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirota, US 5,291, 294 in view of Juen, US 5818,524.**

In regard to claim 8, Hirota, US 5,291, 294, discloses an image processor, comprising:

a solid-state imaging element (see figure 8, element 32) comprising a plurality of light receiving sensors to convert optical signals to electrical signals (see column 6, lines 30-33); and

an electrical signal holder (see figure 8, element 38) within said solid-state imaging element comprising line buffers (see column 6, lines 47-49).

The Hirota reference does not disclose an encoder encoding the electrical signals in units of n.times.m pixels.

Juen, US 5,818,524, discloses a digital still image camera with an irreversible encoder that codes image data before saving onto a recording medium (see figure 2, element 28 and column 4, lines 5-20).

It would have been obvious to one of ordinary skill in the art at the time of invention to have been motivated to modify Hirota, US 5,291, 294 in view of Juen, US 5818,524, to have an encoder encoding the electrical signals in units of n.times.m pixels in order to compress image data output from the image sensor so the more data may be stored on a recording medium.

In regard to claim 9, Hirota, US 5,291, 294 in view of Juen, US 5818,524, discloses the image processor of claim 8, further comprising:

a first switch circuit connecting one of the line buffers and the light receiving sensors (see Hirota: column 6, lines 49-53).

In regard to claim 10, Hirota, US 5,291, 294 in view of Juen, US 5818,524, discloses the image processor of claim 9, wherein data in the line buffers are output in parallel (see Hirota: column 6, lines 60-62).

In regard to claim 11, Hirota, US 5,291, 294 in view of Juen, US 5818,524, discloses the image processor of claim 8, further comprising:

a switch circuit selecting one of the line buffers to output the electrical signal (see Hirota: column 6, lines 60-63: It is inherent that there are switches to control the flow of the signals from each register to the transfer section).

In regard to claim 12, Hirota, US 5,291, 294 in view of Juen, US 5818,524, discloses the image processor of claim 8, wherein said encoder is a JPEG encoder (see Juen: see column 4, lines 13-15).

In regard to claims 13 and 17, Hirota, US 5,291, 294, discloses an image processor and method for operating the processor, comprising:

a solid-state imaging element (see figure 8, element 32) having a plurality of light-receiving sensors to convert optical signals into electrical signals (see column 6, lines 30-33); and

an electrical signal holder (see figure 8, element 38) within said solid-state imaging element comprising a plurality of buffers, each buffer storing m data (see column 6, lines 47-49).

The Hirota reference does not disclose an encoder encoding the electrical signals in units of n.times.m pixels.

Juen, US 5,818,524, discloses a digital still image camera with an irreversible encoder that codes image data before saving onto a recording medium (see figure 2, element 28 and column 4, lines 5-20).

It would have been obvious to one of ordinary skill in the art at the time of invention to have been motivated to modify Hirota, US 5,291, 294 in view of Juen, US 5818,524, to have an encoder encoding the electrical signals in units of n.times.m pixels

in order to compress image data output from the image sensor so the more data may be stored on a recording medium.

In regard to claim 14, Hirota, US 5,291, 294 in view of Juen, US 5818,524, discloses the image processor of claim 13, further comprising:

a switch circuit connecting one of the line buffers and the light receiving sensors (see Hirota: column 6, lines 49-53).

In regard to claim 15, Hirota, US 5,291, 294 in view of Juen, US 5818,524, discloses the image processor of claim 13, further comprising:

a transfer control circuit (see figure 8, element 33) selecting certain ones of the light-receiving sensors to supply an electrical signal to the buffers (see column 6, lines 42-45).

In regard to claim 16, Hirota, US 5,291, 294 in view of Juen, US 5818,524, discloses the image processor of claim 13, wherein said encoder is a JPEG encoder (see Juen: see column 4, lines 13-15).

**8. Claims 20, 23, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirota, US 5,291, 294 in view of Aciu et al., US 5,625,412.**

In regard to claim 20, Hirota, US 5,291, 294 discloses a charge-coupled device (CCD), comprising:

a vertical CCD (see figure 9, element 44) having a plurality of photosensors arranged in v vertical lines and n horizontal lines corresponding to an n.times.v frame of pixels, and converting optical signals to electrical signal image data (see column 7, lines 30-47: When the image senor is rotated by 90

degrees, the element 33 can be read as the Vertical CCD and element 34 as the horizontal CCD);

a horizontal CCD (see figure 9, element 44) having n line buffers (see figure 9, element 47), each buffer holding up to v pixels of image data (see column 7, lines 48-51);

a switch circuit connected to each of the vertical lines and the line buffers (see column 7, lines 51-67); and

a switch control circuit controlling said switch circuit so that each line buffer sequentially connects to said vertical CCD, the image data in sequential ones of the n horizontal lines of said vertical CCD being transferred to a corresponding one of the n line buffers (see column 7, lines 51-67).

The Hirota reference does not disclose the image data in the n line buffers being output in parallel to the external circuit.

Aciu et al., US 5,625,412, discloses a camera with a CCD image sensor that outputs image data in parallel using N outputs (see column 3, lines 22-30 and 39-42). The parallel readout structure maximizes speed and reduces noise (see column 3, lines 23-25).

It would have been obvious to one of ordinary skill in the art at the time of invention to have been motivated to modify Hirota, US 5,291, 294 in view of Aciu et al., US 5,625,412, to have the image data in the n line buffers being output in parallel to the external circuit, in order to maximize the transfer speed.

In regard to claims 23 and 26, Hirota, US 5,291, 294 discloses a charge-coupled device (CCD) and the method of outputting image data from the CCD, comprising:

an array of photosensors arranged in v vertical lines and n horizontal lines corresponding to an n.times.v pixel array of image data (see column 7, lines 30-47: When the image senor is rotated by 90 degrees, the element 33 can be read as the Vertical CCD and element 34 as the horizontal CCD); and

a plurality of n line buffers (see figure 9, element 47), each line buffer holding up to v pixels of image data, wherein each line buffer sequentially connecting to said array (see column 7, lines 48-56), the image data in sequential ones of the n horizontal lines of said array being transferred to a corresponding one of the n line buffers (see column 7, lines 57-67).

The Hirota reference does not disclose the image data in the n line buffers being output in parallel to the external circuit.

Aciu et al., US 5,625,412, discloses a camera with a CCD image sensor that outputs image data in parallel using N outputs (see column 3, lines 22-30 and 39-42). The parallel readout structure maximizes speed and reduces noise (see column 3, lines 23-25).

It would have been obvious to one of ordinary skill in the art at the time of invention to have been motivated to modify Hirota, US 5,291, 294 in view of Aciu et al., US 5,625,412, to have the image data in the n line buffers being output in parallel to the external circuit, in order to maximize the transfer speed.

***Conclusion***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following art discloses solid state imaging devices with memory buffers:

US 5,426,317,

US 5,539,536,

US 5,317,408,

US 4,500,915,

US 4,785,353.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gevell Selby whose telephone number is 703-305-8623. The examiner can normally be reached on 8:00 A.M. - 5:30 PM (every other Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Christensen can be reached on 703-308-9644. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gvs

TUAN HO
PRIMARY EXAMINER